

WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:
 - a memory array including a plurality of memory cells and a plurality
 - 5 of dummy cells;
 - a row decoder connected to the memory array;
 - a dummy control circuit connected to the memory array;
 - a column selector connected to the memory array;
 - an amplifier circuit connected to the column selector;
 - 10 a dummy column selector connected to the memory array; and
 - an amplifier control circuit connected to the dummy column selector
 - and the amplifier circuit,
 - wherein the plurality of dummy cells are arranged as a first dummy
 - column including a first group of the dummy cells placed in a column at a
 - 15 position close to the row decoder in a row direction and a second dummy
 - column including a second group of the dummy cells placed in a column at a
 - position farthest from the row decoder in a row direction, with the plurality of
 - memory cells interposed between the first dummy column and the second
 - dummy column,
 - 20 the dummy control circuit activates the first dummy column and the
 - second dummy column through a first dummy word line and a second dummy
 - word line, respectively
 - the dummy column selector selects either one of a signal on a first
 - dummy bit line connected to the first dummy column and a signal on a second
 - 25 dummy bit line connected to the second dummy column; and
 - the amplifier control circuit generates an amplifier startup signal
 - with respect to the amplifier circuit, based on a signal from the dummy
 - column selector.
- 30 2. The semiconductor memory device according to claim 1, wherein the
- dummy column selector includes a delay adjusting portion for adjusting a
- delay time with respect to signals output from the first and second dummy
- columns.
- 35 3. The semiconductor memory device according to claim 2, wherein the delay
- adjusting portion is composed of a plurality of delay circuits having different
- delay times, and any of the plurality of delay circuits is selected in accordance

with a memory capacity.

4. The semiconductor memory device according to claim 1, wherein the
dummy control circuit outputs a signal for selecting either one of the first
5 dummy column and the second dummy column to the dummy column selector,
and

the dummy column selector includes a first connection selecting
portion for selecting either one of the first dummy column and the second
dummy column, in accordance with a selection signal from the dummy
10 control circuit.

5. The semiconductor memory device according to claim 4, wherein the
dummy control circuit includes a dummy word line driver, a fuse element, a
PMOS transistor, a NMOS transistor, a NMOS transistor for latching, an
15 inverter for outputting, an inverter for inverting a signal, a first AND circuit
for outputting a first active signal to the first dummy column, and a second
AND circuit for outputting a second active signal to the second dummy
column,

the fuse element is connected between a power supply and a source of
20 the PMOS transistor,

a reset signal is supplied to a gate of the PMOS transistor and a gate
of the NMOS transistor,

a drain of the PMOS transistor is connected to a drain of the NMOS
transistor,

25 a source of the NMOS transistor and a source of the NMOS transistor
for latching are grounded,

an input terminal of the inverter for outputting is connected to the
drain of the PMOS transistor, the drain of the NMOS transistor, and a drain
of the NMOS transistor for latching,

30 an output terminal of the inverter for outputting is connected to a
gate of the NMOS transistor for latching, an input terminal of the inverter for
inverting a signal, one input terminal of the second AND circuit, and the
dummy column selector,

an output terminal of the inverter for inverting a signal is connected
35 to one input terminal of the first AND circuit and the dummy column selector,
and

the other input terminals of the first and second AND circuits are

connected to an output terminal of the dummy word line driver.

6. The semiconductor memory device according to claim 4, wherein the dummy column selector includes a delay adjusting portion for adjusting a
5 delay time with respect to signals output from the first and second dummy columns, and a second connection selecting portion for selecting either one of the signals subjected to delay adjustment by the delay adjusting portion in accordance with a selection signal from the dummy control circuit.

10 7. The semiconductor memory device according to claim 1, wherein output signals of the first and second dummy columns are supplied to corresponding first and second amplifier control circuits through the dummy column selector, and

15 the first and second amplifier control circuits output first and second amplifier startup signals to the amplifier circuit, respectively.

8. The semiconductor memory device according to claim 7, wherein the first and second amplifier control circuits respectively include a signal selecting
20 portion for receiving first and second selection signals from the dummy control circuit and selecting whether or not the first and second amplifier startup signals are output to the amplifier circuit.

9. The semiconductor memory device according to claim 7, wherein the first and second amplifier control circuits respectively include a delay adjusting
25 portion for adjusting a delay time with respect to signals from the first and second dummy columns output from the dummy column selector.

10. The semiconductor memory device according to claim 9, wherein the delay adjusting portion includes a plurality of delay circuits having different
30 delay times, and either one of the plurality of delay circuits is selected in accordance with a memory capacity.

11. The semiconductor memory device according to claim 8, wherein the first and second dummy columns respectively include a switching cell configured
35 by using the same element as that of the dummy cell, and
the switching cell switches connection of the plurality of dummy cells in accordance with the first and second selection signals from the dummy

control circuit.

12. The semiconductor memory device according to claim 1, wherein the
5 semiconductor memory device includes a test terminal for checking an output
signal of the amplifier control circuit.

13. The semiconductor memory device according to claim 1, wherein a
plurality of control lines that are output lines of the dummy control circuit
are wired so as to have an equal length on the first and second dummy
10 columns and around the memory array.